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Question Paper Code : 31227

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2012.

Sixth Semester

Electronics and Communication Engineering

EC 1354 — VLSI DESIGN

(Common to Electrical and Electronics Engineering)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare NMOS and PMOS devices.

2. What is meant by body effect?

3. What is inverter ratio?

4. Draw the circuit diagram and briefly explain about the NMOS inverter.

5. Give the expression for rise time and fall time in CMOS inverter circuit.

6. Write an expression for power dissipation in CMOS inverter.

7. What are the different types of CMOS testing?

8. What is delay modeling?

9. What is a task in verilog?

10. Define the syntax for architecture in verilog HDL.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Discuss the small signal model of MOS transistor. (8)

(ii) Explain in detail about the second order effects in the MOS transistors. (8)

Or

(b) (i) With a neat diagram explain the steps involved in the p-well process of CMOS-fabrication. (10)

(ii) Explain the twin tub process with a neat diagram. (6)

12. (a) (i) Explain DC characteristics of CMOS inverter. (10)

(ii) Draw the stick and layout diagram of an NMOS inverter. (6)

Or

(b) (i) Discuss the design techniques to reduce switching activity in a dynamic CMOS circuits. (8)

(ii) Analyze the CMOS inverter circuit which driving the large capacitance loads. (8)

13. (a) Describe in detail about the resistance and capacitance estimation calculation in a CMOS circuit with the proper loads and drivers. (16)

Or

(b) (i) Explain in detail about the scaling concept. (8)

(ii) Discuss about design margining. (8)

14. (a) Explain in detail about binary decoders and priority encoders. (16)

Or

(b) (i) Design a 4 : 1 MUX using transmission gates. (8)

(ii) Construct an 8 : 1 multiplexer using 4 : 1 and 2 : 1 MUX units. (8)

15. (a) (i) Give a verilog structural gate level description of a bit comparator. (10)

(ii) Write the program using verilog HDL to implement a full adder circuit. (6)

Or

(b) (i) Give a verilog structural gate level description of a ripple carry adder. (10)

(ii) Give a brief account of timing control and delay in verilog. (6)

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